ABSTRACT OF THE DISCLOSURE

A method and mechanism for performing branch prediction. A processor is configured with a branch prediction cache which is configured to store branch prediction information corresponding to a group of instructions. Branch marker bits are stored, each of which correspond to a different byte range of a group of instruction bytes. Each branch marker bit provides an indication as to whether or not a predicted branch instruction ends within the corresponding byte range. In response to receiving a fetch address, a corresponding branch marker bit is selected. A determination is made as to whether the selected bit indicates the presence of a predicted branch instruction. A plurality of branch prediction information entries are also maintained. If the selected branch marker bit indicates a predicted branch, the position of the selected branch marker bit relative to other branch marker bits may be used to select a corresponding entry from the branch prediction information entries.